

AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

Please cancel claims 7-13 and 17-20 without prejudice.

1. (PREVIOUSLY PRESENTED) A method of conditional branching in a pipelined processor, the method comprising the steps of:

(A) fetching a first instruction stored at a branch target address in response to encountering a branch instruction at a program counter address;

(B) decoding a second instruction stored at a next address immediately following said program counter address during a same pipeline cycle as said fetching;

(C) evaluating between (i) taking a branch defined by said branch instruction and (ii) not taking said branch during said same pipeline cycle as said fetching; and

(D) fetching a third instruction stored at a mispredict recovery address immediately following said next address in response to determining not to take said branch.

2. (CURRENTLY AMENDED) A The method of conditional branching in a pipelined processor, the method of claim 1, further comprising the steps ~~of~~ step of:

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~~(A) fetching a first instruction stored at a branch
target address in response to encountering a branch instruction at
a program counter address,~~

~~———— (B) decoding a second instruction stored at a next
address immediately following said program counter address during
a same pipeline cycle as with said fetching,~~

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~~———— (C) evaluating between (i) taking a branch defined by
said branch instruction and (ii) not taking said branch during said
same pipeline cycle as said fetching, and~~

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~~———— (D) fetching a third fourth instruction stored at a
sequential instruction address immediately following said branch
target address in response to determining to take said branch.~~

3. (PREVIOUSLY PRESENTED) The method of claim 2,
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further comprising the step of:

generating said sequential instruction address based upon
said program counter address and a predetermined offset.

4. (PREVIOUSLY PRESENTED) The method of claim 1,
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further comprising the step of:

generating said misprediction recovery address based upon
an exception program counter address and a predetermined offset.

5. (PREVIOUSLY PRESENTED) The method of claim 1,
further comprising the step of:

generating said branch target address based upon said
program counter address and an address displacement of said branch
instruction.

6. (CURRENTLY AMENDED) The method of claim 2, further
comprising the steps of:

generating ~~a~~ said sequential instruction address
immediately following said branch target address based upon said
program counter address and a first predetermined offset;

generating ~~a~~ said mispredict recovery address immediately
following said next address based upon an exception program counter
address and a second predetermined offset; and

generating said branch target address based upon said
program counter address and an address displacement of said branch
instruction; ~~and~~

~~fetching a fourth instruction stored at said mispredict
recovery address in response to determining to not take said
branch.~~

7. (CANCELED)

8. (CANCELED)

9. (CANCELED)

10. (CANCELED)

11. (CANCELED)

12. (CANCELED)

13. (CANCELED)

14. (PREVIOUSLY PRESENTED) A pipelined processor comprising:

means for decoding a first instruction stored at a next address immediately following a program counter address;

5 means for fetching a second instruction stored at a branch target address in a same pipeline cycle as said decoding in response to encountering a branch instruction at said program counter address;

10 means for evaluating between (i) taking a branch defined by said branch instruction and (ii) not taking said branch during said same pipeline cycle as said fetching; and

5 means for fetching a third instruction stored at a mispredict recovery address immediately following said next address in response to determining not to take said branch.

15. (CANCELED)

16. (PREVIOUSLY PRESENTED) The method of claim 1,
further comprising the step of:

storing said program counter address for said branch
instruction in a stage of said pipelined processor for at least two
5 pipeline cycles.

17. (CANCELED)

18. (CANCELED)

19. (CANCELED)

20. (CANCELED)